

FUJY 16.847 (100794-09723)
09/460,898REMARKS

This amendment is in response to the Examiner's Office Action dated 3/29/2004 and further in view of the telephone interview of 05/05/2004. Applicants are also appreciative of the professional and courteous interview held with the examiner. Applicants believe that the arguments presented in the interview and the current amendment should obviate outstanding issues and make the pending claims allowable. Reconsideration of this application is respectfully requested in view of the foregoing amendment and the remarks that follow.

STATUS OF CLAIMS

Claims 1-40 are pending.

Claim 23 is withdrawn from consideration.

Claims 1-16, 18-22, and 24-40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chao et al. (USP 6,449,283), in view of Oba et al. (USP 6,262,986).

Claim 17 stands rejected under 35 U.S.C. § 103(a) as being obvious over Chao et al. (USP 6,449,283).

OVERVIEW OF CLAIMED INVENTION

The presently claimed invention provides for a scheduling system that is structured to determine a proper output route based upon a forwarding request given from an input buffer unit and to perform scheduling so that packets forwarded from respective input buffers are routed to different output routes.

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In an exemplary embodiment, the present invention's scheduling control system for a switch having a Virtual Output Queue comprises a request information management unit, an inter-highway pointer, an intra-highway pointer, and a scheduling processing unit. The request information management unit manages a number of scheduling requests and holds forwarding request information of each input line as a scheduling target with respect to a desired output line. The inter-highway pointer control unit indicates a start-of-scheduling input line and the intra-highway pointer control unit indicates a start-of-retrieval output line in the forwarding request information corresponding to each input line. The scheduling processing unit starts the retrieval of the output lines from the output line indicated by the intra-highway pointer control unit according to the forwarding request information, selects the output line unselected by other input lines, performs the scheduling for all the input lines in sequence starting from the input line indicated by the inter-highway pointer control unit, and updates each start-of-retrieval output line indicated by the intra-highway pointer control unit at a next scheduling cycle. The scheduling processing unit executes arbitration such that a scheduling result does not compete between lines.

In the Claims

In the interview of 05/05/2004, the examiner put forth suggestions for amendments for clarifying applicants' invention. Applicants, via the current amendment, have incorporated the examiner's suggestions and believe that based on the amendments, arguments presented during the interview of 05/05/2004, and arguments to follow, the case is in condition for allowance.

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09/460,898REJECTIONS UNDER U.S.C § 103(a)

Claims 1-16, 18-22, and 24-40 stand rejected under U.S.C. § 103(a) as being unpatentable over U.S. patent to Chao (6,449,283), in view of U.S. patent to Oba et al. (6,262,986), hereafter Oba. Claim 17 stands rejected under U.S.C. § 103(a) as being unpatentable over U.S. patent to Chao (6,449,283). To be properly rejected under U.S.C. § 103(a), each and every element of the claims must be addressed through known prior art or be recognized as an obvious variation thereof. Applicants' contend (and as was shown during the interview of 05/05/2004) that the Chao reference, either by itself or in combination with the Oba reference, fails to provide for many of the limitations as required by applicants' claimed invention.

The Oba reference teaches a fair scheduling apparatus comprising a plurality of packet queues for temporarily storing entered packets (wherein a weight is set up for each packet), a packet input means for entering packets into at least one of a plurality of packet queues, scheduling information management means for managing scheduling information for specifying an order to read out packets stored in the queues, according to a queue length of each packet queue and a weight set up for each packet queue; and a packet output means for reading out and outputting desired packets.

It should however be noted (and as was shown in the interview of 05/05/2004) that the scheduler of Oba is on an output line. For support of this argument, applicants respectfully ask the examiner to look at figure 10 and corresponding description in column 13, lines 53+ as it clearly discloses Oba's scheduler on an output line. Hence,

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Oba does not teach handling arbitration between input lines (such as in a input buffer switch). Hence, applicants contend that Oba's scheduling system differs from the present invention's scheduling system, and its purpose, operation, and functionality.

The Chao reference teaches a method and apparatus for providing a fast ring reservation arbitration via a switch with a virtual output queue. Multiple priority levels are disclosed in columns 31 and 32 of the Chao reference. Chao further discloses that priority levels may be considered during arbitration. In stark contrast, the present invention's scheduler manages a number of scheduling requests and performs scheduling from a higher priority class among two or more classes. Column 16, lines 26+ of the Chao reference describes a scheduling algorithm, wherein the algorithm comprises of two phases. In a first request phase, each input arbiter chooses a virtual output queue with a head of line cell and sends a request to an output arbiter. In this phase, one VOQ is selected using a round robin control by input Arbiter from VOQ in a self-line, and a request is notified to output arbiter corresponding to the VOQ). In a second grant phase, each output arbiter chooses a requesting input port and sends a grant signal back. In this phase, one input line is selected by round robin from the received inputs, and the result is notified to output arbiter corresponding to the VOQ (i.e., a request is notified from one input line to only one output line).

In summary, Chao's scheduling method comprises the following steps, implemented within the 1-packet time (see figure a): (a) determine, in a round robin fashion, a forwarding destination of a request in each input arbiter and sends the request

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to an output arbiter, and (b) determine, in a round robin fashion, an input arbiter for giving a grant in each output arbiter and report the result to the input arbiter. It should be noted that the steps (a) and (b) are performed at high-speed during the 1-packet time.

However, depending on a condition of input/output arbiter, it is known that a case of non-scheduling (empty slot) will happen only with the one-scheduling process, irrespective of existence of input lines that expect to output to output ports. To solve this problem, Chao discloses the iSLIP method (see Chao's figure 11, and corresponding description in §1.2.3.1.4 and column 10, lines 51+), wherein the above-mentioned series of processes are repeated N times (see figure b) to improve scheduling performance. The operations of iSLIP can be summarized as follows: (a) sending a request, (b) determining, in a round robin manner, a provisional input arbiter for giving a grant in each output arbiter and report the input arbiter and (c) determining, in a round robin manner, output ports for outputting from a plurality of grants in each input arbiter.

For any scheduling method, it is required to repeat the process N times (1~n) for input arbiter and output arbiter processes (receiving/transmitting requests and grants) within the 1-packet time. In a switching system, accommodating a high-speed line interface, it is necessary to have such a high-speed device because the 1-packet time becomes extremely shortened. In a conventional method, pointers of input/output arbiters are updated based on the result of previous scheduling, and therefore becomes a problem as the next scheduling cannot be performed until a previous scheduling process has completely finished. Thus, it is necessary to have high-speed processes. Therefore,

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in Chao, competition does not occur among the plurality of out arbiters that selects the same input line.

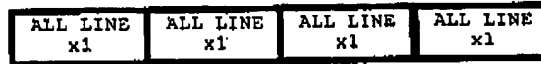


Figure a: Chow's scheduling method

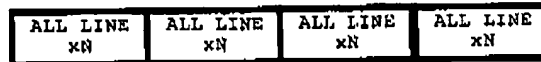


Figure b: iSLIP's scheduling method

wherein each box  = ONE SCHEDULING PROCESSING

Contrastingly, as shown below in figure c, the present invention makes sequentially cycling an input line for starting a scheduling in every scheduling. Thereby, it is possible to perform a next scheduling for the same input line before completing a former scheduling. In other words, it is possible to perform a pipeline process. Therefore, in the present invention, it is possible to perform one scheduling process in N packets (N is a number of lines). However, this scheduling process must be performed a plurality of times.

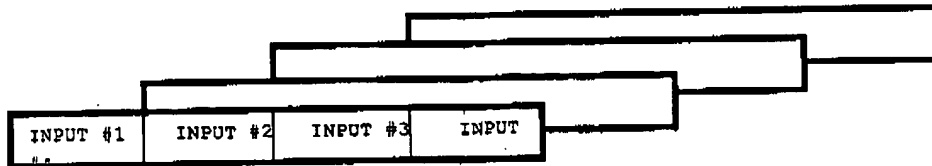


Figure c

Thereby, it is possible to execute scheduling processes with a processing speed that does not depend upon a device capability (see page 5 of the present application as

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filed). If a cycling of input lines is fixed in one direction, impartiality will not be maintained depending on how the lines are aligned. Thus, a mechanism for reversing a cycling order of the input lines is provided so as to realize a high performance.

Thus, as outlined during the interview, both Oba and Chao, either by themselves or in combination, fail to teach at least the following limitations:

- a scheduling process wherein the process aims at executing arbitration so that the scheduling result does not compete between lines
- a scheduling process having competition arbitration between input lines
- a scheduler for managing the number of scheduling requests and performing the scheduling from a higher priority class among two or more classes
- a scheduling process comprising pipeline processing means for independently executing a pipeline process
- a scheduling control system having a schedule processing unit executing arbitration such that a scheduling result does not compete between lines and, wherein , the schedule processing unit further comprises a load observing unit for scheduling a next cycle based on the load
- a switch having a schedule processing unit and a band control unit, wherein the schedule processing unit executes arbitration such that a scheduling result does not compete between lines and the band control unit controls delay and band control of each QoS class in the output line

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- a schedule processing unit having N-pieces of priority patterns with different selection priorities between the respective input lines
- a scheduling processing unit executing arbitration such that a scheduling result does not compete between lines and sequentially performing the scheduling of N-patterns from a priority pattern (indicated by a priority pointer)

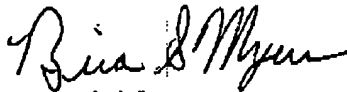
SUMMARY

As has been detailed above and further in view of the interview of 05/05/2004, none of the references, cited or applied, provide for the specific claimed details of applicant's presently claimed invention, nor renders them obvious. It is believed that this case is in condition for allowance and reconsideration thereof and early issuance is respectfully requested.

A petition for extension of time has been filed with this amendment.

If it is felt that an additional interview would expedite prosecution of this application, please do not hesitate to contact applicant's representative at the below number.

Respectfully submitted,



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